Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method in a multi-processor data processing system for managing processors, the method comprising:

responsive to detecting a failed processor in a first set of processors on a first multi-chip module, determining whether a first spare processor from said first set of processors is available to replace said failed processor; ~~identifying a spare processor on the multi-chip module; and~~

in response to determining that said first spare processor is available, assigning the first spare processor to replace the failed processor[[.]];

in response to determining that said first spare processor is unavailable, determining whether a second spare processor from a second set of processors on a second multi-chip module is available to replace said failed processor;

in response to determining that said second spare processor is available, assigning the second spare processor to replace said failed processor; and

simultaneously utilizing said first multi-chip module to execute code for a first operating system and utilizing said second multi-chip module to execute code for a second operating system.

2. (Currently amended) The method of claim 1, wherein the first spare processor and the second spare processor are each ~~on the multi-chip module is~~ marked for use as a spare.

3. (Currently amended) The method of claim 1 further comprising:

assigning said first multi-chip module to a first logical partition of hardware; and

assigning said second multi-chip module to a second logical partition of hardware.

~~selecting another spare processor on a different multi-chip module if the spare processor is absent.~~

4. (Currently amended) The method of claim 1, wherein the first spare processor and the second spare processor are each [[is]] marked by an open firmware.

5-6. (Canceled)

7. (Currently amended) The method of claim 1 [[6]], wherein the failed processor and the first spare processor are included in one die ~~is selected from a die containing the failed processor~~.

8. (Currently amended) A multi-processor data processing system for managing processors, the data processing system comprising:

determining ~~detecting~~ means, responsive to [[for]] detecting a failed processor in a first set of processors on a first multi-chip module, for determining whether a first spare processor from said first set of processors is available to replace said failed processor; ~~identifying a spare processor on the multi-chip module; and~~

in response to determining that said first spare processor is available, assigning means for assigning the first spare processor to replace said failed processor[[.]];

determining means, responsive to determining that said first spare processor is unavailable, for determining whether a second spare processor from a second set of processors on a second multi-chip module is available to replace said failed processor;

assigning means, responsive to determining that said second spare processor is available, for assigning the second spare processor to replace said failed processor; and

utilizing means for simultaneously utilizing said first multi-chip module to execute code for a first operating system and utilizing said second multi-chip module to execute code for a second operating system.

9. (Currently amended) The multi-processor data processing system of claim 8, further comprising marking means for marking the first spare processor and the second spare processor ~~on the multi-chip module~~ for use as a spare.

10. (Currently amended) The multi-processor data processing system of claim 8 further comprising:

said first multi-chip module assigned to a first logical partition of hardware; and

said second multi-chip module assigned to a second logical partition of hardware.

~~selecting means for selecting another spare processor on a different multi-chip module if the spare processor is absent.~~

11. (Currently amended) The multi-processor data processing system of claim 8, further comprising marking means for marking the first spare processor and the second spare processor by an open firmware.

12-13. (Canceled)

14. (Currently amended) The multi-processor data processing system of claim 13, wherein the failed processor and the first spare processor are included in one die. ~~selecting means for selecting the spare processor from a die containing the filed processor.~~

15. (Currently amended) A computer program product in a computer readable medium for managing processors, the computer program product comprising:

first instructions responsive to detecting a failed processor in a first set of processors on a first multi-chip module, for determining whether a first spare processor from said first set of processors is available to replace said failed processor; ~~identifying a spare processor on the multi-chip module; and~~

in response to determining that said first spare processor is available, second instructions for assigning the first spare processor to replace the failed processor[[.]];

in response to determining that said first spare processor is unavailable, third instructions for determining whether a second spare processor from a second set of processors on a second multi-chip module is available to replace said failed processor;

in response to determining that said second spare processor is available, fourth instructions for assigning the second spare processor to replace said failed processor; and

fifth instructions for simultaneously utilizing said first multi-chip module to execute code for a first operating system and utilizing said second multi-chip module to execute code for a second operating system.

16. (Currently amended) The computer program product of claim 15, wherein the first spare processor and the second spare processor are both ~~on the multi-chip module is~~ marked for use as a spare.

17. (Currently amended) The computer program product of claim 15 further comprising:

sixth instructions for assigning said first multi-chip module to a first logical partition of hardware; and

seventh instructions for assigning said second multi-chip module to a second logical partition of hardware.

~~third instructions for selecting another spare processor on a different multi-chip module if the spare processor is absent.~~

18. (Currently amended) The computer program product of claim 15, wherein the first spare processor and the second spare processor are each [[is]] marked by an open firmware.

19-20. (Canceled)

21. (Currently amended) The computer program product of claim 15 [[20]], wherein the failed processor and the first spare processor are included in one die ~~is selected from a die containing the filed processor~~.

22. (New) The method according to claim 1, wherein said first operating system and said second operating system are different types of operating systems.

23. (New) The multi-processor data processing system according to claim 8, wherein said first operating system and said second operating system are different types of operating systems.

24. (New) The computer program product according to claim 15, wherein said first operating system and said second operating system are different types of operating systems.